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(54) **Semiconductor store**

(57) In a semiconductor store comprising a plurality of storage cells each comprising an MOS-selector transitor (AT) which is operated by an operating line (WL) and storage capacitor (CS) which is connected to the selector transistor (AT), a depletion-type varactor is used as the storage capacitor (CS). This reduces the sensitivity of the module to variations in the supply voltage and reduces information loss. If desired, the peripheral load transistors of the store can also be in the form of depletion-type varactors. The depletion-type varactor can be produced either by reducing the thickness of the gate oxide layer (GOS) of the capacitor, or by implanting a conductive channel in the semiconductor substrate surface.

Fig.2

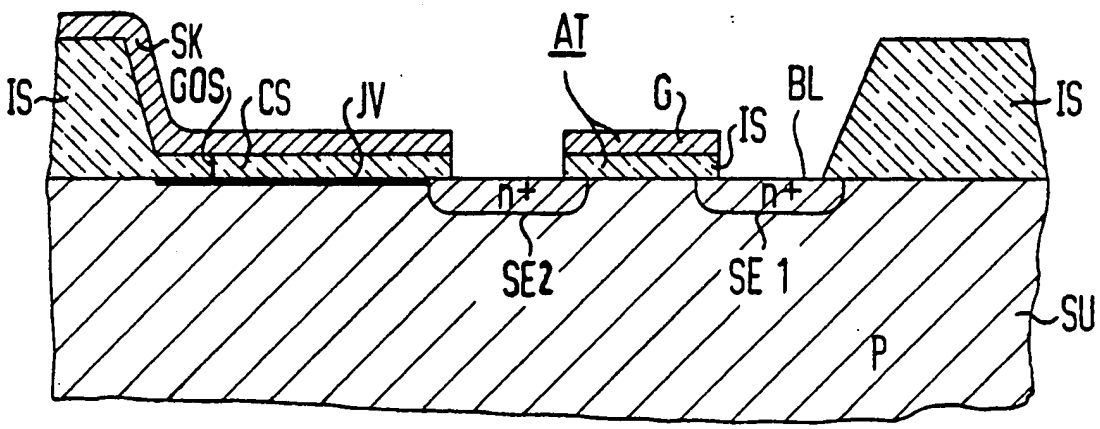

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FIG 1

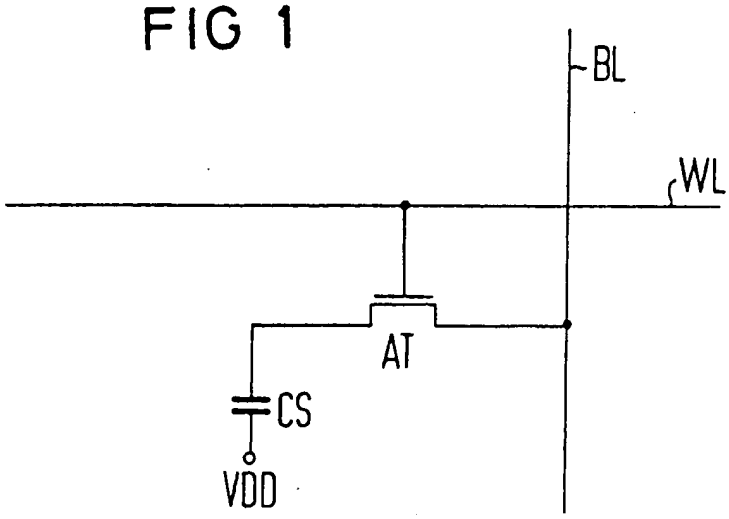
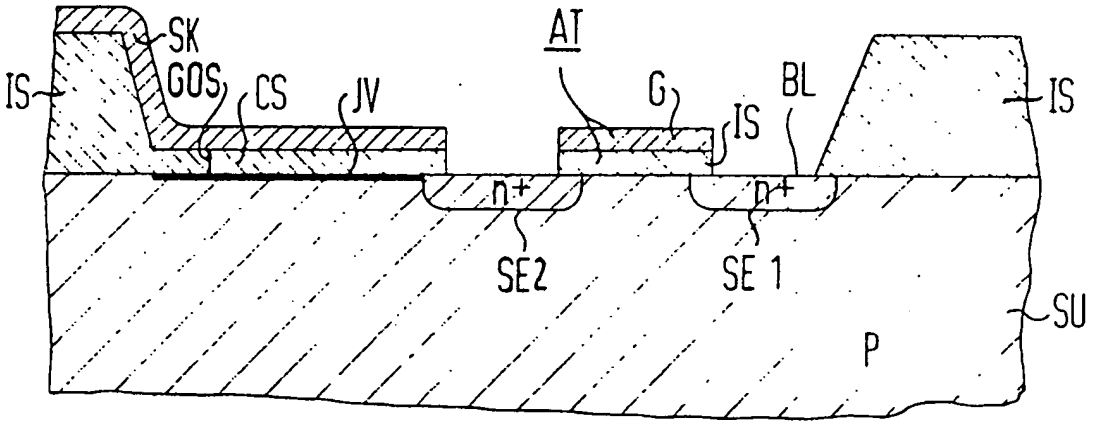


Fig.2



SPECIFICATION

Improvements In or relating to semiconductor stores

The present invention relates to semiconductor stores comprising a plurality of storage cells, each consisting of an MOS-selector transistor which is operated by an operating line of the store and of a storage capacitor which is connected to the selector transistor.

One-transistor storage cells produced by the MOS-technique are known; see, for example, Electronics, Sept. 31, 1973, pp. 116–121. The one-transistor storage cells described in this article consist of a selector transistor and a storage capacitor which is connected to the selector transistor. The control electrode of the selector transistor is connected to a word line of the semiconductor store, while the controlled path of the selector transistor lies between a bit line and one terminal of the storage capacitor. The other terminal of the capacitor is maintained at a fixed voltage VDD. The information which is to be stored in the storage cell is defined by the charge of the storage capacitor. The write-in and readout of an item of information into and from the storage cell is effected via the selector transistor, if the latter is operated by the word line.

In highly integrated dynamic MOS-storage modules of this kind, the capacitors storing the information are preferably designed as MOS-varactors using the n–Si–gate, or n–Si^2-gate-technology. Usually, the highest operating voltage of, for example, 12 volts, which prevails in the module is applied to the gate-electrode of these varactors i.e. is the voltage VDD. This leads to the fact that with every alteration of the operating voltage, the stored information can be affected directly via the gate capacitance and indirectly via word lines which are inadmissably raised. Both effects, together or individually, break down the stored information to such an extent that an unambiguous read-out operation is no longer possible.

The sensitivity of available MOS-storage modules to variations in supply voltage cannot readily be reduced because of the design of the storage capacitor as an enhancement-type varactor and because of a permissible fluctuation of ± 10% in the value of the voltage VDD is a normal design requirement. The sensitivity of such known modules to supply voltage variation can be reduced by the provision of additional circuitry if, for example, during the operating phase of the module during write-in or read-out operations, the operating voltage in the cell field is isolated from the operating voltage of the periphery of the store, i.e. if the gate electrodes of all the cell varactors "float" for a short time.

However, this isolation process cannot be extended to the cycle pause because the drop in level of the gate electrodes of the cell field, which always occur because of the inevitable leakage currents, must be compensated. Thus, as before, changes in operating voltages during such pauses are disturbing, even in the case of this mode of operation.

It is an object of the present invention to provide a semiconductor store having storage cells containing MOS-varactors, which are such that only a low operating voltage is necessary, so that disturbance of the stored information by fluctuations in the operating voltage is substantially lower than in the known stores of this type.

According to the invention, there is provided a semiconductor store comprising a plurality of storage cells each comprising an MOS-selector transistor adapted to be operated by an operating line and a storage capacitor which is connected ato the selector transistor and is in the form of a depletion-type MOS-varactor.

Such a depletion-type varactor can advantageously be produced by reducing the thickness of the gate-oxide layer in the varactor region a value of 300 to 500 Å, and/or by producing an electrically conductive channel is produced by ion implantation in the varactor region.

The invention will now be further described with reference to the drawing, in which:–

Figure 1 is a basic circuit diagram of a one-transistor storage cell formed using this MOS-technique; and

Figure 2 is a schematic side-sectional view of a one-transistor storage cell according to the invention, produced in the n-channel-silicon-gate technique.

The basic MOS-one-transistor storage cell shown in Fig. 1 comprises a selector transistor AT and a storage capacitor CS. The storage cell is arranged between a word line WL and a bit line BL. The gate electrode of the selector transistor AT is connected to the word line WL whilst the controlled path of the selector transistor AT lies between the bit line BL and one terminal of the storage capacitor CS. The other terminal of the storage capacitor CS is connected to a fixed voltage VDD. The charge which characterises an item of information is stored in the storage capacitor CS. This charge can be transferred to the bit line BL via the selector transistor AT. This takes place when the word line WL is appropriately operated.

Fig. 2 shows such a one-transistor storage cell produced in accordance with the known n-channel-silicon-gate-technique. The storage capacitor CS and the selector transistor AT are arranged beside one another on a p-doped silicon semiconductor substrate SU having a doping concentration of about 10^{16} atoms/cm^3. The two controlled electrodes SE1 and SE2 of the selector transistor are in the form of n^+ doped zones having a doping

concentration of about 10^{24} atoms/cm^3, diffused into the semiconductor substrate SU. The gate electrode G of the transistor AT is arranged between the controlled electrodes SE1 and SE2 and partially overlaps these electrodes, the gate being insulated from the semiconductor substrate SU by a gate insulation layer IS. The one controlled electrode SE1 forms part of the bit line BL. The other controlled electrode SE2 is connected to the storage capacitor CS. The latter is formed by means of a conductor path SK which is arranged above the semiconductor substrate SU and separated therefrom by a gate insulation layer GOS. If an appropriate voltage is applied to the conductor path SK, an inversion layer IV which is connected to the controlled electrode SE2 of the selector transistor AT, is formed at the surface of the semiconductor substrate SU. The insulating layers GOS and IS which are required for the formation of the storage capacitor CS and the selector transistor AT respectively, may consist of silicon oxide. The gate electrode G of the selector transistor AT can consist of polycrystalline silicon.

In known forms of storage cell of this type, the storage capacitor CS is a so-called enhancement-type varactor in which the inversion layer IV does not form until a high voltage (e.g. of 12 volts) has been applied to the conductor path SK.

If, however, in accordance with the invention, a depletion-type varactor is used in place of the known enhancement-type varactor, substantially improved operation is obtained. Advantageously, this depletion-type varactor can be formed by reducing the thickness of the gate oxide layer GOS to a value of 300 to 500 Å. If, in this case, the conductor path SK is connected to the ground potential 0 volt which is one supply potential of the storage module, a thin inversion layer IV is formed by virtue of the surface charges which always exist in the substrate SU. The use of a thin gate oxide layer leads to a relatively high capacitance of the storage capacitor CS.

The same effect can be achieved by implanting ions into the surface of the semiconductor substrate SU so as to produce a stable inversion layer IV.

By using a depletion-type varactor, the ground operating voltage 0 which prevails in the module can be used for the gate-electrodes of the varactors. The earth line is not subject to any fluctuations so that the security of the stored information in the storage capacitor CS is substantially increased.

If desired, the reduction in the gate oxide thickness and/or the use of channel implantation proposed for the cell field can also be used in the load transistors (resistors) of the periphery of the module. Thus, these load transistors can likewise be designed in the depletion mode, whereby the operating speed of the module is increased and the number of the operating voltages necessary reduced. In particular, the use of an operating voltage of about 12 volts can be given up.

CLAIMS

1. A semiconductor store comprising a plurality of storage cells each comprising an MOS-selector transistor adapted to be operated by an operating line and a storage capacitor which is connected to the selector transistor and is in the form of a depletion-type MOS-varactor.

2. A semiconductor store as claimed in Claim 1, wherein said depletion-type varactor comprises an oxide layer of thickness 300 to 500 Å arranged on a doped semiconductor substrate and a gate electrode on said oxide layer adapted to be connected in use to the ground potential of the store.

3. A semiconductor store as claimed in Claim 1 or Claim 2 wherein an electrically conductive channel is produced in the surface of said substrate in the region of the varactor by means of ion implantation.

4. A semiconductor store as claimed in any one of Claims 1 to 3, wherein all the load transistors of said store are formed as depletion-type transistors.

5. A semiconductor store as claimed in Claim 1 substantially as hereinbefore described with reference to the drawing.

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